IN THE CLAIMS

Please amend the claim as follows:

1. (Currently Amended) A precoder comprising:

a judgment unit ~~for~~ configured to judge~~ing~~ whether an odd number or even number of '1's exists in data input signals of N channels inputted at an n^{th} time of channel input;

a toggle unit ~~for~~ configured to toggle~~ing~~ an output signal of the judgment unit when said number of '1's is judged by the judgment unit to be odd, said ~~toggling~~ toggle unit determining an output value of a channel of the N channels; and

communicatively connected to the toggle unit, an output unit ~~for~~ configured to determine~~ing~~ output values of other channels of the N channels according to respective ones of the data input signals.

2. (Original) The precoder as claimed in claim 1, wherein the judgment unit includes a plurality of exclusive OR gates connected to each other in a pyramid configuration, so that the judgment unit outputs to the toggle unit '0' when said number of '1's is judged by the judgment unit to be even, or '1' when said number of '1's is judged by the judgment unit to be odd.

3. (Currently Amended) The precoder as claimed in claim 2, wherein the output unit includes N-1 XOR gates ~~for~~ configured to ~~sequentially~~ perform~~ing~~ ~~an~~ XOR operations sequentially, each operation having ~~that has~~ as an input a respective one of said input signals and ~~that has~~ having as a further input a signal representative of a respective one of the channel output values.

4. (Currently Amended) The precoder as claimed in claim 3, wherein the toggle unit comprises:

an AND gate ~~for~~ configured to ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) ~~for~~ configured to toggling an output signal of the AND gate at each rising edge of the output signal of the AND gate.

5. (Currently Amended) The precoder as claimed in claim 2, wherein the output unit includes N-1 XOR gates ~~for~~ configured to perform~~ing~~ XOR operations, each operation having as an input a respective one of said input signals and further having as an input a signal representative of a respective one of the channel output values.

6. (Currently Amended) The precoder as claimed in claim 5, wherein the toggle unit comprises:

an AND gate ~~for~~ configured to perform ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) ~~for~~ configured to toggle~~ing~~ an output signal of the AND gate at each rising edge of the output signal of the AND gate.

7. (Currently Amended) The precoder as claimed in claim 2, wherein the toggle unit comprises:

an AND gate ~~for~~ configured to perform ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) ~~for~~ configured to toggle~~ing~~ an output signal of the AND gate at each rising edge of the output signal of the AND gate.

8. (Currently Amended) The precoder as claimed in claim 1, wherein the toggle unit comprises:

an AND gate ~~for A~~ configured to perform ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) ~~for~~ configured to toggle~~ing~~ an output signal of the AND gate at each rising edge of the output signal of the AND gate.

9. (Currently Amended) The precoder as claimed in claim 1, wherein the output unit includes N-1 XOR gates ~~for~~ configured to ~~sequentially~~ perform~~ing~~ ~~an~~ XOR operations sequentially, each operation having that has as an input a respective one of said input signals and that has as a further input a signal representative of a respective one of the channel output values.

10. (Currently Amended) The precoder as claimed in claim 9, wherein the toggle unit comprises:

an AND gate ~~for~~ configured to perform ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) ~~for~~ configured to toggle~~ing~~ an output signal of the AND gate at each rising edge of the output signal of the AND gate.

11. (Currently Amended) The precoder as claimed in claim 1, wherein the output unit includes N-1 XOR gates ~~for~~ configured to perform~~ing~~ XOR operations, each operation having as an input a respective one of said input signals and further having as an input a signal representative of a respective one of the channel output values.

12. (Currently Amended) The precoder as claimed in claim 11, wherein the toggle unit comprises:

an AND gate ~~for~~ configured to perform ANDing said output signal of the judgment unit and a clock signal; and

a T flip-flop (T-FF) ~~for~~ configured to toggle~~ing~~ an output signal of the AND gate at each rising edge of the output signal of the AND gate.

13. (Withdrawn) A precoder for coding data input signals of N channels inputted at an n^{th} time of channel input, said precoder operating according to the equations:

$$b_{Nn+1} = a_{Nn+1} \oplus b_{Nn}$$
$$b_{Nn+2} = a_{Nn+2} \oplus b_{Nn+1}$$
$$b_{Nn+3} = a_{Nn+3} \oplus b_{Nn+2} \quad ,$$
$$\cdots$$
$$b_{Nn+N} = a_{Nn+N} \oplus b_{Nn+(N-1)}$$

wherein a_{Nn+k} represents input data of an k^{th} of said N channels, b_{Nn+k} represents an output signal of the precoder for the k^{th} of said N channels, and $\oplus$ represents an exclusive OR operation.

14. (Withdrawn) The precoder as claimed in claim 13, wherein the precoder comprises:

N number of XOR gates for receiving the data signals a_{Nn+1} to a_{Nn+N}, respectively; and

a delayer connected to an output terminal of an N^{th} XOR gate,

wherein an output signal of the delayer is fed back to a first one of the N gates, to which the data signal a_{Nn+1} is inputted.

15. (Withdrawn) The precoder as claimed in claim 14, wherein the N is 4.

16. (Currently Amended) An optical duo-binary transmission apparatus comprising:

a precoder ~~for~~ configured to code~~ing~~ in parallel data input signals of N channels; and

a multiplexer ~~for~~ configured to time division multiplex~~ing~~ the signals coded by the precoder.

17. (Currently Amended) The optical duo-binary transmission apparatus as claimed in claim 16, wherein the precoder comprises:

a judgment unit ~~for~~ configured to judge~~ing~~ whether an odd number or even number of '1's exists in data input signals of N channels inputted at an n^{th} time of channel input;

a toggle unit ~~for~~ configured to toggle~~ing~~ an output signal of the judgment unit when said number of '1's is judged by the judgment unit to be odd, said toggle unit ~~ing~~ determining an output value of a channel of the N channels; and

communicatively connected to the toggle unit, an output unit ~~for~~ configured to determine~~ing~~ output values of other channels of the N channels according to respective ones of the data input signals.

18. (Original) The optical duo-binary transmission apparatus as claimed in claim 16, wherein the precoder further comprises a unit to which the data input signals serve as input, said unit being comprised of m stages of XOR gates wherein $N = 2^m$.

19. (Original) The optical duo-binary transmission apparatus as claimed in claim 18, wherein the precoder further comprises an output unit having N-1 stages of XOR gates.

20. (Currently Amended) The optical duo-binary transmission apparatus as claimed in claim 19, wherein the units comprised on m stages ~~is~~ are joined to the output unit by an AND gate feeding a T flip-flop (T-FF).